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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/830,217	04/23/2004	Parthasarathy Ranganathan	200403365-1	9027

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
CONNOLLY, MARK A	
ART UNIT	**PAPER NUMBER**
2115	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/830,217	RANGANATHAN, PARTHASARATHY	
	Examiner	Art Unit	
	Mark Connolly	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/18/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,12,13,18,21-23,26,27 and 29-36* is/are rejected.

7)☒ Claim(s) *3,6-11,14-17,19,20,24,25 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-34 have been presented for examination.

2. Applicant's arguments with respect to claims 23 and 26-27 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 29-33 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. In particular, the claims comprise "software embedded on a computer readable medium" which is defined in the specification as including signals [page 24 lines 13-15]. Therefore the claims are not tangible and therefore not statutory.

For examination purposes, the claims are being interpreted as being embedded a computer readable storage medium.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2, 29-30 and 35-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Evoy et al. [Evoy] US Pat No. 5958055.

7. Referring to claim 1, Evoy teaches the method of selecting I/O devices to control power consumption of a computer system comprising:

a. determining a power consumption metric for each of a plurality of I/O devices connected to the computer system [col. 2 lines 44-56].

b. selecting at least one of the plurality of I/O devices based on the determined power consumption metric [col. 2 lines 44-56].

c. reducing power consumption of the at least one selected I/O device [col. 2 lines 44-56].

In particular, Evoy teaches a power management unit (PMU) for powering off the most energy intensive component of a computer first. Evoy explains that a device, which consumes the most power in one computer system, does not necessarily consume the most power in another. Therefore, in order to identify which component uses the most power, it is inherent that the PMU must be able to determine each devices power usage.

8. Referring to claim 2, Evoy teaches powering off the device that uses the most power [col. 2 lines 52-56].

9. Referring to claims 29 and 30, these are rejected on the same basis as set forth hereinabove. Evoy teaches the method and therefore teaches the computer software performing the method.

10. Referring to claims 35 and 36, Evoy teaches the I/O device as being a monitor which as is well known, receives data from an operating system for display [col. 2 lines 52-54].

11. Claims 23, 26 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Frantz et al. [Frantz] US Pat No 5557557.

12. Referring to claim 23, Frantz teaches method including:

d. profiling usage patterns of the I/O devices to establish a usage model [col. 7 lines 26-29 and 35-41].

e. identifying low-power alternatives to using at least one of the I/O devices using the usage model [col. 5 lines 9-21 and col. 7 lines 30-55].

f. profiling power consumption of the I/O devices to establish a power model [col. 7 lines 35-48].

g. selecting at least one of the low power alternatives to reduce power consumption of the computer system based on the power model [col. 7 lines 49-55].

In summary, the Frantz system teaches comprising a plurality of processing units wherein the above method for determining the necessary power for executing a plurality of instructions with respect to the instructions usage of the processor is applied to a selected processor. Therefore, since different processing units can be selected, it is inherent that the method is applied to the plurality of processing units.

13. Referring to claim 26, this is rejected on the same basis as set forth hereinabove. Frantz teaches the method and therefore teaches the apparatus performing the method.

14. Referring to claim 27, Frantz teaches performing substantially the same function at reduced power consumption [col. 3 lines 4-6 and 41-55].

15. Claims 1-2, 12-13, 18, 21-22 and 29-30 are rejected under 35 U.S.C. 102(a) as being anticipated by Orenstien[1].

16. Referring to claim 1, Orenstien teaches the method of selecting I/O devices to control power consumption of a computer system comprising:

h. determining a power consumption metric for each of a plurality of I/O devices connected to the computer system [col. 3 lines 10-11, col. 4 line 67- col. 5 line 4].

i. selecting at least one of the plurality of I/O devices based on the determined power consumption metric [col. 5 lines 16-20]. Swapping processes from a processor consuming a large amount of power is interpreted as selecting that processor to swap its processes.

j. reducing power consumption of the at least one selected I/O device [col. 7 lines 5-8]. A processor swapping out its high power process for a low power process reduces the power consumption of the processor.

17. Referring to claim 2, Orenstien teaches monitoring the power consumption of a plurality of processing units [col. 3 lines 3-14]. In addition, Orenstien further analyzes the power consumption for each processing unit to determine if the power consumption between the units is uneven (i.e. which units are consuming more power than others) [col. 3 lines 35-39]. This inherently identifies top power consuming processing units which then swap their high power processes with a low power processes thus reducing the processing units power consumption [col. 3 lines 54-57 and col. 7 lines 5-8].

[1] As cited in the previous office action.

18. Referring to claim 12, Orenstein teaches the power consumption metric, which is used to select a processing unit may comprise both a power consumption value and operational activity [col. 3 lines 17-27].

19. Referring to claim 13, Orenstein teaches determining an aggregate power consumption [col. 6 lines 46-54].

20. Referring to claims 18 and 21, Orenstein teaches a power consumption metric for each I/O device comprising an operational activity, which is obtained from polling the I/O devices, and is used to select a processing unit [col. 3 lines 17-50]. In addition, Orenstein also teaches profiling power consumption of the devices, and generating a model in which to use in selecting one of the devices [col. 4 line 67-col. 5 line 4 and col. 5 lines 16-20]. Calculating a plurality of power consumption metrics including averaged and integrated power over time for each processor is interpreted as generating a power model and because the model also includes simple and complex activity factors (i.e. processor usage), the power model is also interpreted as being a usage model as well.

21. Referring to claims 22 and 29-30, these are rejected on the same basis as set forth hereinabove. Orenstein teaches the method and therefore teaches the program performing the method.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 4-5 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orenstein as applied to claims 1-2, 12-13, 18, 21-22 and 29-30 above, and further in view of Cai[2].

24. Referring to claim 4, although Orenstein teaches the invention substantially above, it is not explicitly taught to identify low-power alternatives to using the top power consuming devices. In summary, Orenstein does not explicitly teach using lower power devices in place of higher power consuming devices in order to reduce power consumption. Rather, Orenstein teaches a means in which a processor can be throttled [col. 6 lines 46-54]. Cai teaches a system comprising a plurality of processors, each with different power consumption levels wherein a lower power processor is selected to execute instead of a higher power processor in order to reduce power [col. 1 lines 41-54]. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Orenstein to substitute a lower power processor for use instead of a higher power processor instead of throttling in order to further reduce power as taught in Cai [col. 1 lines 55-56].

25. Referring to claim 5, Cai teaches placing a top power consuming I/O device in a low power mode [col. 3 lines 55-58].

26. Referring to claim 34, Orenstein teaches determining power consumption metrics for each of a plurality of I/O devices as shown above. Orenstein further teaches operating only one processor "when battery power falls below a selected threshold" [col. 8 lines 2-6]. Cai teaches using the lowest power processor during a battery-operating mode allows for extended operating time [53-58]. It is obvious that the Orenstein-Cai system would examine the power consumption

of each processor and select only the most adequate power efficient processor to execute when the battery falls below the threshold. Since only the power efficient processor is executing, it is interpreted that the other processors are in a reduced power consumption state.

Allowable Subject Matter

27. Claims 3, 6-11, 14-17, 19-20, 24-25 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

28. Claims 31-33 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 101, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

29. Applicant's arguments with respect to claims 1-2, 4-5, 12-13, 18, 21-22, 29-30 and 34 filed 18 December 2006 have been fully considered but they are not persuasive.

30. In the REMARKS, applicant argues in substance that 1) Orenstein discloses a plurality of processing units rather than a plurality of I/O devices 2) a multi-core processor is a computer system and therefore cannot be connected to a computer system 3) Orenstein does not fails to teach identifying top power consuming I/O devices 4) Orenstein does not disclose generating a model from profiling device power consumption and usage 5) Orenstein fails to teach reducing power consumption in response to remaining battery life falling below a threshold.

In response to arguments 1 and 2, it is not unreasonable to interpret a processor or a group of processors as being I/O devices. Are they not devices? Do they not input and output

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[2] As cited in the previous office action.

data? An I/O device, broadly speaking, is a device that accepts input data in addition to outputting data, which is exactly what processors do. Furthermore, despite applicant's belief, a processor alone is not a computer system. Although it may be part of the computer system, it alone does not make up the entire system. If a person wanted to buy a new processor for their computer, they would not go to the local computer store and ask the sales person for a computer system. If they did, they would be offered something like a desktop PC or a laptop computer, not a standalone processor. A computer system is made up of a bunch of components including a processor(s), memory, hard drive, motherboard, peripheral I/O devices, etc... which are all connected to each other. Therefore, connecting a processor to the plurality of devices that make up a computer system inherently connects the processor(s) to the computer system.

In response to argument 3, Orenstien analyzes the power consumption for each processing unit to determine if the power consumption between the units is uneven (i.e. which units are consuming more power than others) [col. 3 lines 35-39]. This inherently identifies top power consuming processing units which then swap their high power processes with a low power processes thus reducing the processing units power consumption.

In response to argument 4, Orenstein teaches gathering information necessary to select a processor. Included in this information are power metrics such as average power for each processing unit using measured values which are based on activity of the processors, interpreted as the usage, and are presented as a composite of the above factors in addition to several other factors for measuring and estimating power consumption [col. 3 lines 10-27, col. 4 line 67-col. 5 line 4 and col. 5 lines 16-20]. Calculating the power consumption metrics over time based on activity for each processor is interpreted as generating a model representing power and usage.

In response to argument 5, Orenstein explicitly teaches only operating a single processor "when *battery power falls below a selected threshold*" [*emphasis added* col. 8 lines 2-6].

Conclusion

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (571) 272-3666. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mark Connolly
Examiner
Art Unit 2115

mc
March 9, 2007